Notice of Allowability	Application No.	Applicant(s)	
	10/626,636	PARK ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed 10/4/2007 and interview on 11/13/2007*.

2. ☒ The allowed claim(s) is/are *1,2 and 5-17*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 10/4/2007, with respect to claims 1, 2, 6, 8, 9, 15-17 have been fully considered and are persuasive. The rejection of claims 1, 2, 6, 8 & 9 has been withdrawn.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with **Robert Goodell** (Reg. No. 41,040) on 11/13/2007.

The application has been amended as follows:

In the claims:

(Please note that amendments are shown in underline, strikethrough and/or double square brackets)

Claim 1 (currently amended) A memory providing apparatus for an image data interpolation in an image processing system having an image sensor outputting line image data from a sensed image, comprising:

a readable and writable single memory;

a buffer register having a prior data area storing first line image data, which has been stored in the memory, in a unit of ~~2-m~~ 2m bits, and having a present data area storing second line image data, which is inputted in a unit of m bits, in a unit of the ~~2-m~~ 2m bits; and

a memory controller providing the memory with a chip enable signal, a write enable signal, and an address indicating locations of the first and second line image data stored in the buffer register, reading and writing the first and second line image data from and on the memory, and outputting the first and second line image data and a third line image data, which is inputted from the image sensor wherein the memory comprises a ~~4-m~~ 4m bits memory cell having upper and lower areas storing in a memory cell unit of ~~2-m~~ 2m bits data, respectively, which are readable and writable by the memory controller, and wherein the memory controller controls the chip enable signal and the write enable signal to be enabled and disabled, respectively, and reads the first line image data from the memory when the chip enable signal and the write enable signal are enabled and disabled, respectively, to store the first line image data in the prior data area of the buffer register, and the memory controller controls the chip enable signal and the write enable signal to be enabled, and stores the first and second line image data, which have been stored in the buffer register, in the memory in a unit of the memory cell unit.

Claim 7 (currently amended) A memory providing apparatus for an image data interpolation in an image processing system having an image sensor outputting line image data from a sensed image, comprising:

a readable and writable single memory;

a buffer register having a prior data area storing first line image data, which has been stored in the memory, in a unit of ~~2-m~~ 2m bits, and having a present data area storing second line image data, which is inputted in a unit of m bits, in a unit of the ~~2-m~~ 2m bits;

a memory controller providing the memory with a chip enable signal, a write enable signal, and an address indicating locations of the first and second line image data stored in the buffer register, reading and writing the first and second line image data from and on the memory, and outputting the first and second line image data and a third line image data, which is inputted from the image sensor; and

an image signal processor performing a 3x3 line interpolation using the first, second, and third line image data; and

first, second, and third data transmission lines through which the first, second, and third line image data are outputted from the memory controller, respectively,

wherein the memory controller reads the first and second line image data stored in the memory, transmits the first and second line image data through the first and second data transmission lines, and transmits the third line image data, which is inputted directly from the image sensor, through the third data transmission line according to a same clock.

Claim 8 (currently amended) The apparatus of claim 1, wherein the first, second and third line image data [[comprises:]] comprise a Bayer pattern.

Claim 9 (currently amended) The apparatus of claim 1, wherein the image sensor comprises: one of a charge coupled device image sensor and a complementary metal oxide semiconductor.

Claim 10 (currently amended) A method of providing line data for interpolation in an image processing system, the method comprising:

storing first line image data outputted from an image sensor in a unit of m bits in a present data area of a buffer register in a unit of ~~2-m~~ 2m bits;

storing the first line image data of the present data area of the buffer register in a memory in the unit of the ~~2-m~~ 2m bits;

refreshing the buffer register;

reading the first line image data from the memory in the unit of the ~~2-m~~ 2m bits to store the read first line image data in a prior data area of the buffer register, and storing second line image data outputted from the image sensor in the unit of the m bits in the present data area of the buffer register in the unit of the ~~2-m~~ 2m bits;

storing the first line image data and the second line image data stored in the prior data area and the present data area of the buffer register, respectively, in the memory in a unit of ~~4-m~~ 4m bits; and

transmitting the first and second line image data stored in the memory and third line image data outputted directly from the image sensor to an image signal processor .according to a same clock signal.

Claim 11 (currently amended) The method of claim 10, wherein the transmitting of the first, second, and third line image data comprises: reading the first line image data stored in the memory using a memory [[controller-connected]] controller connected to the memory; reading the second line image data stored in the memory using the memory controller; and outputting the third line image data inputted from the image sensor and the first and second line image sensor to the image signal processor through respective data transmission lines.

Claim 15 (currently amended) The apparatus of claim 7, wherein the memory comprises a ~~4-m~~ 4m bits memory cell having upper and lower areas storing in a memory cell unit of ~~2-m~~ 2m bits data, respectively, which are readable and writable by the memory controller.

Claim 16 (currently amended) The apparatus of claim 7, wherein the first, second and third line image data ~~comprises~~ comprise a Bayer pattern.

Allowable Subject Matter

3. Claims 1, 2 and 5-17 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art of record fails to teach or fairly suggest the combination of all limitations of claim 1 that includes **"the memory controller controls the chip enable signal and the write enable signal to be enabled and disabled, respectively, and reads the first line image data from the memory when the chip enable signal and the write enable signal are enabled and disabled, respectively, to store the first line image data in the prior data area of the buffer register, and the memory controller controls the chip enable signal and the write enable signal to be enabled, and stores the first and second line image data, which have been stored in the buffer register, in the memory in a unit of the memory cell unit."**

Regarding claim 7, the prior art of record also fails to teach or fairly suggest the combination of all limitations of claim 7 that includes **"first, second, and third data transmission lines through which the first, second, and third line image data are outputted from the memory controller, respectively, wherein the memory controller reads the first and second line image data stored in the memory, transmits the first and second line image data through the first and second data transmission lines, and transmits the third line image data, which is inputted directly from the image sensor, through the third data transmission line according to a same clock."**

Regarding claim 10, the prior art of record also fails to teach or fairly suggest the combination of all limitations of claim 10 that includes **"storing the first line image data of the present data area of the buffer register in a memory in the unit of the 2m bits; refreshing the buffer register; reading the first line image data from the memory in the unit of the 2m bits to store the read first line image data in a prior data area of the buffer register, and storing second line image data outputted from the image sensor in the unit of the m bits in the present data area of the buffer register in the unit of the 2m bits; storing the first line image data and the second line image data stored in the prior data area and the present data area of the buffer register, respectively, in the memory in a unit of 4m bits; and transmitting the first and second line image data stored in the memory and third line image data outputted directly from the image sensor to an image signal processor according to a same clock signal."**

Regarding claims 2, 5, 6, 8 & 9, these claims are allowed as being dependent from claim 1.

Regarding claims 15-17, these claims are allowed as being dependent from claim 7.

Regarding claims 11-14, these claims are allowed as being dependent from claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner